

**IN THE UNITED STATES  
PATENT AND TRADEMARK OFFICE**

**Patent Application****Inventor(s)** Shrenik Deliwala**Case** 053168-500301D6**Conf. No.** 1405**Serial No.** 10/079,668**Group Art Unit** 2874**Filing Date** February 20, 2002**Examiner** Michelle R. Connelly-Cushwa**Title** Hybrid Active and Electronic Circuit with Evanescent Coupling

**COMMISSIONER OF PATENTS  
WASHINGTON, D.C. 20231**

**SIR:**

**AMENDMENT**

In response to the Office action dated February 28, 2003 (application Paper No. 10), please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please amend the paragraph beginning at line 19 of page 129 as follows:

---FIGs. 69, 70 and 71 show three other embodiments of hybrid active electronic and optical circuits 6502. FIGs. 69, 70, and 71 are each top views of their respective devices. The basic purpose of each of the hybrid active electronic and optical circuits 6502 shown in FIGs. 69, 70, and 71 is to couple light from a relatively wide (i.e., greater than 100  $\mu\text{m}$ ) input waveguide 6901 into a relatively narrow (i.e., less than 3  $\mu\text{m}$ ) waveguide 6904. ~~The tapered~~ A gap region 6906b is used to evanescently couple light into waveguide 6904. The three FIGs. 69, 70, and 71 show three different ~~techniques~~ passive optical elements that may be used to accomplish the task of changing the direction of incident light within relatively wide input waveguide 6902 into an angle suitable for evanescent coupling into relatively narrow waveguide 6904. These deflection angles can be computed using computational tools such as FDTD.---

Please amend the paragraph beginning at line 2 of page 130 as follows:

---In the embodiment of FIG. 69, ~~deviation~~ deflection is due to a grating 6902 being integrated into the Si layer during manufacture. In the case of FIG. 70, a waveguide prism 7002 created by altering the effective mode index of the Si layer in a manner such that the shape of a prism is created. In the embodiment of FIG. 71, a waveguide lens 7102 is used. The relatively narrow waveguide 6904 may contain an active optical device.---

Please amend the paragraph beginning at line 6 of page 130 as follows:

---During (or before/after) the deposition of the desired silicon and electrical insulators in the active electronic portion 6504, the optical insulator materials are deposited in ~~the an~~ an insulator strip 6906a and evanescent coupling region 6906b. In accordance with the present invention, evanescent coupling region 6906b may be formed to include a tapered gap portion, or a uniformly shaped gap portion, and may comprise a thickness on the order of 0.5  $\mu\text{m}$ . Similarly, the etching of the silicon material for, and deposition of the desired material to form, the active electronic portion 6504 can occur simultaneously with the corresponding etching and deposition of the materials to form the

passive optical portion 6506. The waveguide 6904 may additionally be considered as a passive optical portion.---

Please amend the paragraph beginning at line 13 of page 130 as follows;

---The embodiment of hybrid active electronic and optical circuit 6502 shown in FIG. 69 includes a waveguide grating 6902 to couple impinging light from relatively wide input waveguide 6901 into the relatively narrow waveguide 6904 through evanescent coupling region 6906b. The waveguide grating 6902 is configured such that impinging light 6920 from relatively wide input waveguide 6901 is deflected at a suitable angle so the deflected light 6922 enters the relatively narrow waveguide 6904 at a suitable mode angle  $\theta_M$ . The waveguide grating 6902 is a passive optical portion 6506, and can be controlled by active electronics 6504 to control the angle of deflection, as described herein. Alternatively, the waveguide grating 6902 can be configured as a purely passive device that deflects the light being applied to the waveguide 6904 to the mode angle.---

Please amend the paragraph beginning at line 21 of page 130 as follows:

---FIG. 70 shows another embodiment of hybrid active electronic and optical circuit 6502 shown in FIG. 69, except that the waveguide prism 7002 has been incorporated in place of the waveguide grating 6902. Similarly, the waveguide prism 7002 is a passive device, that deflects the light being applied to the waveguide 6904 in a mode angle  $\theta_M$ . The use of the active electronic component 6504 allows adjustability of the light flowing through the waveguide prism 7002, thereby allowing light flowing through the waveguide prism 7002 to be controllably directed at a desired controllable angle to the relatively narrow waveguide 6904.---

Please amend the paragraph beginning at line 3 of page 131 as follows:

---The material of waveguide prism 7002, the active electronic portion 6504, ~~and~~ the insulator strip 6906a and evanescent coupling region 6906b can all be etched, and the corresponding layers deposited, simultaneously. Different photoresists and masks may allow different materials to be deposited in each of the areas being etched, however, a

sequence of all the deposition steps and etching steps that comprise all the processes performed on all of the optical portions and electronic portions, may be performed simultaneously. If a specific material is being deposited on one portion (but not another), or etched on one portion (but not another), then the corresponding masks and etching or deposition tools will be configured accordingly. FIG. 71 shows another embodiment of hybrid active electronic and optical circuit 6502 in which full waveguide lens 7102 is formed in the upper most silicon layer of the SOI wafer 6600 in place of the waveguide prism 7002 shown in the embodiment of FIG. 70.---

IN THE CLAIMS:

12. *(currently amended)* A hybrid active electronic and optical circuit integrated within a Silicon-On-Insulator (SOI) wafer, the SOI wafer including an insulator layer and an upper silicon layer having a thickness of less than 3  $\mu\text{m}$ , the hybrid active electronic and optical circuit comprising:

a relatively narrow waveguide located within the upper silicon layer of the SOI wafer for supporting the propagation of light, said relatively narrow waveguide having a thickness of less than 3  $\mu\text{m}$ ;

an active electronic circuit positioned proximate the waveguide, wherein a flow of light through the waveguide can be altered depending on a property of the active electronic circuit;

a light deflector at least partially located in the upper silicon layer, the light deflector is configured to deflect light impinging at the suitable incident angle to a suitable mode angle where light deflected by the light deflector enters the relatively narrow waveguide; and

an evanescent coupling region at least partially located within the upper silicon layer, the evanescent coupling region including a gap region positioned between the light deflector and the relatively narrow waveguide for optically couples coupling the deflected light coupling portion into the waveguide, such that light emitted from the light deflector coupling portion can pass via the evanescent coupling gap region to the relatively narrow waveguide at a suitable mode angle; and

~~—— a light deflector at least partially located in the upper silicon layer, the light deflector is configured to deflect light impinging at the suitable incident angle to a suitable mode angle where light deflected by the light deflector enters the waveguide.~~

13. – 14. *cancelled*

15. *(currently amended)* The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling gap region includes a substantially constant thickness gap portion.

16. *(currently amended)* The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling gap region ~~is at least partially formed using an optically clear adhesive~~ includes a tapered gap portion.

**17. cancelled**

18. *(original)* The hybrid active electronic and optical circuit of claim 12, further including at least one optical device, wherein altering an electric voltage applied to the active electronic circuit affects a free carrier distribution in a region of the at least one optical device, and thereby changes an effective mode index of the at least one optical device.

**19. cancelled.**

20. *(currently amended)* The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling gap region has a thickness of less than  $0.5\mu\text{m}$ .

**21. – 28. cancelled**

29. *(original)* The hybrid active electronic and optical circuit of claim 12, wherein the hybrid active electronic and optical circuit includes a Fabry-Perot cavity.

30. *(original)* The hybrid active electronic and optical circuit of claim 12, wherein the hybrid active electronic and optical circuit includes a wavelength division multiplexer modulator.

31. *(original)* The hybrid active electronic and optical circuit of claim 12, wherein the hybrid active electronic and optical circuit includes a diode.

32. *(original)* The hybrid active electronic and optical circuit of claim 12, wherein the hybrid active electronic and optical circuit includes a transistor.

**33. – 36. cancelled**

37. *(original)* The hybrid active electronic and optical circuit of claim 12, wherein the hybrid circuit includes one from the group of a p-n device, a field plated device, a Schottky device, a MOSCAP, and a MOSFET.

38. *(currently amended)* A hybrid active electronic and optical circuit integrated within a wafer, the wafer including an insulator layer and an upper silicon layer, the hybrid active electronic and optical circuit comprising:

a waveguide located within the upper silicon layer of the SOI wafer for supporting the propagation of light;

an active electronic circuit positioned proximate the waveguide, wherein a flow of light through the waveguide can be altered depending on a property of the active electronic circuit;

a light deflector at least partially located in the upper silicon layer, the light deflector configured to deflect light impinging at the suitable incident angle to a suitable mode angle where light deflected by the light deflector enters the relatively narrow waveguide; and

an evanescent coupling region at least partially located within the upper silicon layer, the evanescent coupling region including a gap region positioned between the light deflector and the relatively narrow waveguide for optically couples coupling the deflected light coupling portion into the waveguide, such that light emitted from the light deflector coupling portion can pass via the evanescent coupling gap region to the relatively narrow waveguide at a suitable mode angle; and

~~—— a light deflector at least partially located in the upper silicon layer, the light deflector is configured to deflect light impinging at the suitable incident angle to a suitable mode angle where light deflected by the light deflector enters the waveguide.~~

39. (new) The hybrid active electronic and optical circuit of claim 12, wherein the light deflector comprises an optical grating formed in the upper silicon layer.

40. (new) The hybrid active electronic and optical circuit of claim 12, wherein the light deflector comprises an optical prism formed in the upper silicon layer.

41. (new) The hybrid active electronic and optical circuit of claim 40 wherein the light deflector comprises regions of different effective mode indices to create a prism-like region in the upper silicon layer.

42. (new) The hybrid active electronic and optical circuit of claim 12, wherein the light deflector comprises an optical lens formed in the upper silicon layer.

***Remarks***

Reconsideration of remaining claims 12, 15-16, 18, 20, 29-32, 37-38 is respectfully requested. Applicant also requests consideration of newly-submitted claims 39-42.

In the Office action dated February 28, 2003 (application Paper No. 10), the Examiner rejected various combinations of the pending claims under 35 USC §§ 112, second paragraph, 102(b), 102(e) and 103(a). The Examiner's various rejections will be addressed below in the order appearing in the Office action.

***Election/Restriction***

Applicant confirms the election of claims 12, 15-16, 18, 20, 29-32, 37-38. As stated by the Examiner in the Action dated November 26, 2002, claims 12 and 28 are defined as "generic" claims, and the allowability of the remaining, non-elected claims will be re-considered upon allowance of claims 12 and 28.

***Drawings***

As requested by the Examiner, formal drawing sheets for the approved drawing corrections are being filed with this response.

***35 USC § 112, second paragraph Rejection – Claims 12, 15-20, 28-32 and 37***

The Examiner first rejected the above-cited claims under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the present invention. In particular, the Examiner cited the term "the light coupling portion" as recited at line 8 of claim 12 as lacking proper antecedent basis. In response, applicant has amended claim 12 to remove any recitation of a "light coupling portion. Claim 20 was cited by the Examiner as including the phrase "thickness of less than 0.5 $\mu$ ", where the symbol " $\mu$ " is considered to be insufficient in defining a thickness value. In response, applicant has amended claim 20 to recite "0.5 $\mu$ m" and believe that claim 20 is now in condition for allowance.



In light of the amendments to claims 1 and 20, applicant respectfully requests the Examiner to reconsider the 35 USC 112, second paragraph rejections and find claims 1 and 20, as well as claims 15, 16, 18 and 29-32,37 which respectively depend therefrom, to be in condition for allowance.

***35 USC § 102(b) Rejection – Claims 12, 17, 20, 28, 30, 31, 32 and 38***

The above-cited claims were rejected by the Examiner under 35 USC 102(b) as being anticipated by US Patent 4,966,430 (Weidel). In response, applicant has amended independent claim 12 and asserts that Weidel does not disclose, suggest, or anticipate any use of “evanescent coupling” for “optically coupling the deflected light into the waveguide, such that light emitted from the light deflector can pass via the evanescent coupling gap region to the relatively narrow waveguide at a suitable mode angle”, as defined by amended claim 12. Weidel discloses the use of traditional optical waveguides (such as waveguide 5) to support the propagation of light, where the waveguides are of a size such that a mirrored surface (mirror 8) of Weidel can merely redirect propagation of light from an optical transducer 7 into waveguide 5.

In contrast, the arrangement of the present invention is related to optical transmission within a relatively thin (e.g. less than 3  $\mu\text{m}$ ) waveguide along a surface of an SOI structure. The use of an SOI structure, with a waveguide formed in a “thin upper silicon layer” is also not disclosed in Weidel, as that structure is defined in the specification. Lastly, independent claim 12 defines the use of a “light deflector” that is “configured to deflect light impinging at the suitable incident angle to a suitable mode angle where light deflected by the light deflector enters the relatively narrow waveguide”, where embodiments of this deflector may comprise a grating, prism or coupling lens.

Based on these differences, therefore, applicant respectfully requests the Examiner to reconsider this rejection and find remaining claims 12, 20, 3-32 and 38 to be in condition for allowance.

***35 USC § 102(b) Rejection – Claims 12, 15, 18, 19, 28, 31, 32, 37 and 38***

The Examiner next rejected the above-cited claims under 35 USC 102(b) as anticipated by US Patent 5,502,779 (Magel). As with the Weidel reference, applicant asserts that Magel does not disclose or suggest the use of “evanescent coupling” as that term is defined by the rejected claims. Nor is there any disclosure in Magel regarding the use of a “light deflector” to “deflect light impinging at the suitable incident angle to a suitable mode angle where light deflected by the light deflector enters the relatively narrow waveguide”. The structure of Magel includes a relatively wide waveguide 20, where evanescent coupling at the proper “mode angle” is not a concern.

Applicant therefore respectfully requests the Examiner to reconsider this rejection and find remaining claims 12, 15, 18, 31, 32, 37 and 38 to be in condition for allowance.

***35 USC § 102(e) Rejection – Claims 12, 15, 18, 19, 28-30, 37 and 38***

Claims 12, 15, 18, 19, 28-30, 37 and 38 were next rejected by the Examiner under 35 USC 102(e) as being anticipated by US Patent 6,393,169 (Paniccia et al.). As with the above references, applicant asserts that Paniccia et al. discloses an optical structure that utilizes conventional optical coupling techniques, in this case, allowing an incoming light signal to pass through an opening (or via) 821 before impinging a “deflector” 825. Waveguide 897 of Paniccia et al. is disclosed as a conventional, relatively wide waveguide, capable of supporting many signal modes. In contrast, the use of the relatively narrow waveguide of the invention as defined by rejected independent claim 12 requires “evanescent coupling” as the method to couple the optical energy out of the “input” waveguide and into the “narrow” waveguide. The arrangement of Paniccia et al. cannot support such a coupling requirement.

Applicant therefore respectfully requests the Examiner to reconsider this rejection and find remaining claims 12, 15, 18, 29, 30, 37 and 38 to be in condition for allowance.

**35 USC § 103(a) Rejection – Claim 16**

The Examiner next rejected claim 16 under 35 USC 103(a) as being unpatentable over Paniccia et al., as above, where the Examiner cited regions 821 and 823 as being likened to the “evanescent coupling region” defined by rejected claim 12 (from which claim 16 depends). In response, applicant asserts that regions 821 and 823 are simply “optical conduits” that do not effect the angular displacement of a propagating wave and cannot be found to disclose or suggest the phenomena of “evanescent coupling” as that term is known and used in the present specification and rejected claims. Without this teaching, Paniccia et al. cannot be found to render obvious the subject matter of claim 16. Applicant therefore respectfully requests the Examiner to reconsider this rejection and find claim 16 to be in condition for allowance.

**Summary**

Each of the Examiner’s rejections has now been responded to and applicant requests the Examiner to reconsider the various rejections. If the Examiner believes that an interview or telephone conversation would further the prosecution of this application, the Examiner is invited to contact applicant’s attorney at the telephone number listed below.

Respectfully submitted,

Shrenik Deliwala

By: Wendy W. Koba  
Wendy W. Koba  
Reg. No. 30509  
Attorney for applicant  
610-346-7112

Date: 7/24/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Shrenik Deliwala :  
Serial No.: Not yet known : Attorney Docket No.: 53168-500301D6  
Filed: February 20, 2002 :  
For: INTEGRATED OPTICAL/ELECTRONIC :  
CIRCUITS AND ASSOCIATED :  
METHODS OF SIMULTANEOUS :  
GENERATION THEREOF :

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

Dear Sir:

Prior to the examination of this matter, please amend this application as follows:

EXPRESS MAIL CERTIFICATE (37 C.F.R. § 1.10)

Express Mail Label No. EL931061738US

Date of Deposit February 20 2002

I hereby certify that this paper, and the papers and/or fees referred to herein as transmitted, submitted or enclosed, are being deposited with the U.S. Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Name Daniel H. Golub

Signature 

## IN THE CLAIMS

Please delete claims 1-11 and add new claims 12-38 as follows:

12. A hybrid active electronic and optical circuit integrated within a Silicon-On-Insulator (SOI) wafer, the SOI wafer including an insulator layer and an upper silicon layer, the hybrid active electronic and optical circuit comprising:

a waveguide located within the upper silicon layer for receiving light;

an active electronic circuit positioned proximate the waveguide, wherein a flow of light through the waveguide can be altered depending on a property of the active electronic circuit;

an evanescent coupling region at least partially located within the upper silicon layer, the evanescent coupling region optically couples the light coupling portion to the waveguide, light emitted from the light coupling portion can pass via the evanescent coupling region to the waveguide at a suitable angle; and

a light deflector at least partially located in the upper silicon layer, the light deflector is configured to deflect light impinging at the suitable incident angle to a suitable mode angle wherein light deflected by the light deflector enters the waveguide.

13. The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling region includes a tapered gap portion.

14. The hybrid active electronic and optical circuit of claim 13, wherein the tapered gap portion enhances coupling efficiency.

15. The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling region includes a substantially constant thickness gap portion.

16. The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling region is at least partially formed using an optically clear adhesive.

17. The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling region is at least partially formed from air.

18. The hybrid active electronic and optical circuit of claim 12, further including at least one optical device, wherein altering an electric voltage applied to the active electronic circuit affects a free carrier distribution in a region of the at least one optical device, and thereby changes an effective mode index of the at least one optical device.

19. The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling region is at least partially formed from an optically clean polymer.

20. The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling region has a thickness of less than  $0.5\mu$ .

21. The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling region includes a waveguide prism.

22. The hybrid active electronic and optical circuit of claim 13, wherein the evanescent coupling region includes a waveguide prism.

23. The hybrid active electronic and optical circuit of claim 15, wherein the evanescent coupling region includes a waveguide prism.

24. The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling region includes a waveguide grating.

25. The hybrid active electronic and optical circuit of claim 13, wherein the evanescent coupling region includes a waveguide grating.

26. The hybrid active electronic and optical circuit of claim 15, wherein the evanescent coupling region includes a waveguide grating.

27. The hybrid active electronic and optical circuit of claim 12, wherein the hybrid active electronic and optical circuit includes a focusing mirror.

28. The hybrid active electronic and optical circuit of claim 12, wherein the hybrid active electronic and optical circuit includes an input/output coupler that couples light into or out of the waveguide.

29. The hybrid active electronic and optical circuit of claim 12, wherein the hybrid active

electronic and optical circuit includes a Fabry-Perot cavity.

30. The hybrid active electronic and optical circuit of claim 12, wherein the hybrid active electronic and optical circuit includes a wavelength division multiplexer modulator.

31. The hybrid active electronic and optical circuit of claim 12, wherein the hybrid active electronic and optical circuit includes a diode.

32. The hybrid active electronic and optical circuit of claim 12, wherein the hybrid active electronic and optical circuit includes a transistor.

33. The hybrid active electronic and optical circuit of claim 12, wherein the waveguide is at least partially formed using a plurality of electric insulator strips.

34. The hybrid active electronic and optical circuit of claim 12, wherein the light deflector includes a waveguide grating.

35. The hybrid active electronic and optical circuit of claim 12, wherein the light deflector includes a waveguide prism.

36. The hybrid active electronic and optical circuit of claim 12, wherein the light deflector includes a lens.



37. The hybrid active electronic and optical circuit of claim 12, wherein the hybrid circuit includes one from the group of a p-n device, a field plated device, a Schottky device, a MOSCAP, and a MOSFET.

38. A hybrid active electronic and optical circuit integrated within a wafer, the wafer including an insulator layer and an upper silicon layer, the hybrid active electronic and optical circuit comprising:

a waveguide located within the upper silicon layer for receiving light;

an active electronic circuit positioned proximate the waveguide, wherein a flow of light through the waveguide can be altered depending on a property of the active electronic circuit;

an evanescent coupling region at least partially located within the upper silicon layer, the evanescent coupling region optically couples the light coupling portion to the waveguide, light emitted from the light coupling portion can pass via the evanescent coupling region to the waveguide at a suitable angle; and

a light deflector at least partially located in the upper silicon layer, the light deflector is configured to deflect light impinging at the suitable incident angle to a suitable mode angle  $\theta_M$  wherein light deflected by the light deflector enters the waveguide.

#### **IN THE DRAWINGS**

Applicant respectfully requests the Examiner's approval of the proposed changes to the drawing figures 5, 13, 20, 21, 22, 30, 47, 51, 52, 59, 60, 68A, 68B, 68C, 68D, 73, 74, 75, 76, 77, 78, 82, 83 and 88 in the request for Approval of Drawing Changes filed concurrently herewith.

### **IN THE SPECIFICATION**

Rewrite the title on page 1, that starts on line 1 and ends on line 2 to read as follows.

HYBRID ACTIVE AND ELECTRONIC CIRCUIT WITH EVANESCENT COUPLING

Rewrite the paragraph on page 1, that starts on line 5 and ends on line 6 to read as follows.

This application is a divisional of U.S. Patent Application Serial No. 09/991,542, filed November 10, 2001, which is a continuation-in-part of U.S. Patent Application Serial No. 09/859,693, filed May 17, 2001. U.S. Patent Application Serial No. 09/991,542 claims priority to U.S. Provisional Application No. 60/293,615, filed May 25, 2001 and U.S. Provisional Application No. 60/297,208, filed June 8, 2001.

Please delete the paragraph on page 1, that starts on line 7 and ends on line 8.

Please delete the paragraph on page 1, that starts on line 9 and ends on line 10.

Rewrite the paragraph on page 4, that starts on line 17 and ends on line 22 to read as follows.

FIGs. 15A to 15D show side cross section views of the optical waveguide device of FIG. 13 or taken through sectional lines 15-15 in FIG. 13, FIG. 15A shows both gate electrodes 1304,

1306 being deactivated, FIG. 15B shows the gate electrode 1304 being actuated as the gate electrode 1306 is deactivated, FIG. 15C shows the gate electrode 1304 being deactivated as the gate electrode 1306 is activated, and FIG. 15D shows both gate electrodes 1304 and 1306 being actuated;

Rewrite the paragraph on page 9, that starts on line 7 and ends on line 8 to read as follows.

FIGs. 63A to 63D show a method of fabricating the partially completed integrated optical/electronic circuit of FIG. 51;

Rewrite the paragraph on page 9, that starts on line 9 and ends on line 10 to read as follows.

FIG. 64 shows a plot of intensity versus distance from a ledge of one embodiment of input/output light coupler 112 including a tapered gap portion;

Rewrite the paragraph on page 9, that starts on line 11 and ends on line 12 to read as follows.

FIG. 65 shows another plot of intensity at a prism base for another embodiment of input/output light coupler having a prism, but without a tapered gap portion;

Please delete the paragraph on page 9, that starts on line 13 and ends on line 14.

Rewrite the paragraph on page 9, that starts on line 15 and ends on line 16 to read as follows.

FIG. 66 shows one embodiment of hybrid active electronic and optical circuit that is configured as a J-coupler;

Please delete the paragraph on page 9, that starts on line 17 and ends on line 18.

Rewrite the paragraph on page 9, that starts on line 21 and ends on line 21 to read as follows.

FIGs. 68A to 68D show one embodiment of a method of anisotropically etching using a mask.

Rewrite the paragraph on page 12, that starts on line 16 and ends on line 19 to read as follows.

Actual embodiments of discrete optical waveguide devices are described in the “Specific Embodiments of Optical Waveguide Device” portions of this disclosure. More complex optical circuits including a plurality of optical waveguide devices 100 are described in the “Optical Circuits Including Optical Waveguide Devices” portion of this disclosure.

Rewrite the paragraph on page 13, that starts on line 16 and ends on line 25 to read as follows.

FIGs. 51 to 52 show one embodiment of an integrated optical/electric circuit 103. Multiple embodiments of integrated optical/electric circuit 103 are described herein as being formed using SOI devices, etc. The integrated optical/electric circuit can be configured with and combination of active optical, passive optical, active electronics, and passive components circuit. SOI technology is highly promising for integrated optical/electronic circuits, and using relatively thin SOI devices (having an upper silicon layer less than 10  $\mu$ ) has many benefits. Using thin SOI devices for waveguides limits the vertical locations in which light can diffract, and therefore acts to localize the light to a relatively narrow waveguide. Thin SOI devices can be formed using planar lithography techniques including deposition and etching processes.

Rewrite the paragraph that starts on page 16, line 10 and continues over to page 17, line 1 to read as follows.

The embodiments of optical waveguide device 100 shown in multiple figures including FIGs. 1-3, and 5, etc. include a field effect transistor (FET) portion 116 that is electrically coupled to a waveguide 106. One embodiment of the waveguide is fabricated proximate to, and underneath, the gate electrode of the FET portion 116. The waveguide 106 is typically made from silicon or another one or plurality of III-V semiconductors. The FET portion 116 includes a first body contact electrode 118, a gate electrode 120, and a second body contact electrode 122.

A voltage can be applied by e.g., a voltage source 202 to one of the electrodes. The gate electrode 120 is the most common electrode in which the voltage level is varied to control the optical waveguide device. If the first body contact portion 118 and the second body contact portion are held at the same voltage by placing an electrical connector 204 there between, then the optical waveguide device 100 operates as a diode. If there is not an electrical connector between the first body contact portion 118 and the second body contact portion 122, then the optical waveguide device 100 acts as a transistor. This is true for each of the following FET/diode configurations. Whether any FET optical waveguide device 100 is biased to act as a transistor or diode, the optical waveguide device 100 is within the intended scope of the present invention since either a diode or a transistor is capable of altering the effective mode index in the waveguide as described herein.

Rewrite the paragraph on page 67, that starts on line 9 and ends on line 24 to read as follows.

FIG. 30 shows another embodiment of an optical waveguide device 100 including a grating 3008 that is used as a lens to focus light passing through the waveguide. The embodiment of optical waveguide device 100, or more particularly the FIG. 2 embodiment of gate electrode of the optical waveguide device, is modified by replacing the continuous gate electrode (in FIG. 2) with a discontinuous electrode in the shape of a grating (shown in FIG. 30). The grating 3008 is formed with a plurality of etchings 3010 that each substantially parallels the optical path 101 of the optical waveguide device. In the FIG. 30 embodiment of grating 3008, the thickness of the successive etchings 3010 to collectively form gate electrode 120 increases

toward the center of the optical waveguide device, and decreases toward the edges 120a, 120b of the gate electrode 120. Therefore, the region of changeable propagation constant 190 in the waveguide is thicker at those regions near the center of the waveguide. Conversely, the region of changeable propagation constant 190 becomes progressively thinner at those regions of the waveguide near edges 120a, 120b. The propagation constant is a factor of both the volume and the shape of the material used to form the gate electrode. The propagation constant is thus higher for those regions of changeable propagation constant closer to the center of the waveguide.

Rewrite the paragraph that starts on page 84, line 24 and continues over to page 85, line 10 to read as follows.

The high propagation constant bands 4502 correspond to the location of the input mirror gate electrodes 4402 or the output mirror gate electrodes 4404. The low propagation constant bands 4504 correspond to the bands between the input mirror gate electrodes 4402 or the output mirror gate electrodes 4404. The high propagation constant bands 4502 and the low propagation constant bands 4504 extend vertically through the waveguide. The input mirror gate electrodes 4402 and the output mirror gate electrodes 4404 can be shaped to provide, e.g., a concave mirror surface if desired. Additionally, deactuation of the input mirror gate electrodes 4402 or the output mirror gate electrodes 4404 removes any effect of the high propagation constant bands 4502 and low propagation constant bands 4504 from the waveguide of the resonator 4400. Such effects are removed since the propagation constant approaches a uniform level corresponding to 0 volts applied to the gate electrodes 4402, 4404.

Rewrite the paragraph on page 89, that starts on line 17 and ends on line 23 to read as follows.

The wavelength separator 3902 acts to filter or modulate the wavelength of an incoming signal over waveguide 3916 into a plurality of light signals. Each of these light signals has a different frequency. Each of a plurality of waveguides 3918a to 3918d contain a light signal of different wavelength  $\lambda_1$  to  $\lambda_n$ , the wavelength of each signal corresponds to a prescribed limited bandwidth. For example, waveguide 3918a carries light having a color corresponding to wavelength  $\lambda_1$ , while waveguide 3918b carries a light having a color corresponding to wavelength  $\lambda_2$ , etc.

Rewrite the heading on page 100, line 12 to read as follows.

#### VI. Generalization of Active Optical Devices in SOI

Rewrite the heading on page 101, line 4 to read as follows.

#### VII. INPUT/OUTPUT COUPLING EMBODIMENTS

Rewrite the paragraph on page 105, that starts on line 5 and ends on line 19 to read as follows.



It is envisioned that the levels of silicon layers of the on-chip electronics portion 5101 are formed simultaneously with the one or more layers of the evanescent coupling region 5106, (or the gap portion ), and/or the light coupling portion 5110 of the input/output light coupler 112. In other words, any pair of vertically separated layers on the on-chip electronics portion 5101 may be formed simultaneously with any portion of optical elements 5106, 5110 that is at substantially the same vertical level using, for example, planar lithography or projection lithography techniques. Therefore, any one of the one or more layers of the evanescent coupling region 5106 and/or the light coupling portion 5110 that are at generally the same vertical height as the layers on the electronics portion 5101 will be formed simultaneously, although the different portions will undergo different doping, masking, ion implantation, or other processes to provide the desired optical and/or electronic characteristics. As such, technology, know how, processing time, and equipment that has been developed relative to the fabrication of electronic circuits (e.g., techniques for fabricating thin SOI semiconductor chips) can be used to construct optical and electronic circuits simultaneously on the same substrate.

Rewrite the paragraph on page 108, that starts on line 11 and ends on line 23 to read as follows.

The embodiment of input/output light coupler 112 shown in FIG. 55 includes a ledge 5502 that forms a support base for one edge of the light coupling portion 5110 (e.g., a prism or grating). The ledge 5502 may have thickness that provides the desired angle of the base of the input/output light coupler 112. The ledge 5502 is preferably formed by removing sacrificial material at the optical I/O location using an etching process, and the base of the light coupling

portion 5110 is angled at a slight angle by resting it on the ledge 5502. In certain embodiments, the height of the ledge 5502 is in the range of under fifty microns, and may actually be in the range of one or a couple of microns. The gap portion 5106 may be filled with such optically clear polymer or glass material that provides the desired optical characteristics to the light entering into, or exiting from, the waveguide. Light rays 5120 passing through the embodiment of input/output light coupler 112, shown in the embodiment of FIG. 55, must satisfy the basic principles described relative to FIG. 51, e.g., equation 23.

Rewrite the paragraph on page 112, that starts on line 8 and ends on line 24 to read as follows.

As light is exiting the output coupler from the waveguide, wherein the waveguide is carrying substantially uniform intensity of light across the cross-sectional area of the waveguide, it may be desired to once again convert the light exiting the output coupler into a light beam that has a Gaussian intensity profile. Evanescent couplings configured as a tapered gap portion 5106 as illustrated particularly in FIGS. 55 and 57, result in a closer fit to a Gaussian profile than without the taper gap portion. For example, FIG. 64 shows the calculations for a 0.2 micron silicon waveguide formed with the taper. The tapered gap portion is illustrated by line 6402 in FIG. 64, and the height of the taper from the waveguide is illustrated along the right ordinate of FIG. 64. An intensity profile curve 6406 is plotted to indicate the intensity profile at the base of the input/output light coupling device. The relative intensity value is plotted as the left ordinate in FIG. 64. The abscissa measures the distance from a ledge (an arbitrary measuring point) in microns. A best fit Gaussian curve 6404 is plotted proximate the intensity profile 6406, to

illustrate how effectively the output light from the output coupler models the Gaussian curve. FIG. 65 shows a similar curve as FIG. 64, except FIG. 65 models a constant thickness gap, as indicated by the fact that the taper curve 6410 is level in FIG. 65. Curve 6412 of FIG. 65 measures the intensity profile for an output beam of light that is not Gaussian, but instead exponential.

Rewrite the paragraph that starts on page 119, line 18 and continues over to page 120, line 6 to read as follows.

FIGS. 63A to 63D, show a process of simultaneously depositing silica, other suitable dielectric, polysilicon, etc. layer on both the light coupling portion 5110 and the electronic portion 5101. Initially, a silicon layer 6302 is deposited somewhat uniformly across the entire integrated optical/electrical circuit 103, including both the electronics portion 5101 and the light coupling portion 5110. Both the embodiments of the light coupling portion that may include prisms, as well as gratings, rely upon homogenous build up of silica throughout the entire light coupling portion. By comparison, the electronics portion 5101 is formed using a series of silica layers, interspersed with metallic interconnects through which metallic vias vertically extend. Therefore, a series of additional metalization and other steps are necessary between successive depositions of silica. By comparison, since the light coupling portion is homogenous, relatively little processing will occur between the various silica deposition steps. In FIG. 63A, the layer of silicon 6302 is deposited on the upper surface of the integrated optical/electrical circuit 103 using known silicon deposition techniques, such as chemical vapor deposition and sputtering.

Rewrite the paragraph on page 120, that starts on line 7 and ends on line 15 to read as follows.

The planer lithography method continues in FIG. 63B in which a photoresist layer 6304 is deposited on the upper surface of the deposited silicon layer 6302. Photoresist may be applied, and then the substrate 102 typically spun so that the photoresist layer is extended under the influence of centrifugal force to a substantially uniform thickness. In FIG. 63C, the lithography portion 6308 selectively applies light to the upper surface of the photoresist layer 6304, thereby acting to develop certain regions of the photoresist layer. Depending upon the type of photoresist, the photoresist may harden either if light is applied to it, or will not harden if light is not applied. The lithography portion 6308 includes a lithography light source 6310 and a lithography mask 6312.

Rewrite the paragraph that starts on page 120, line 23 and continues over to page 121, line 8 to read as follows.

The photoresist layer 6304 is then washed, in which the undeveloped portions of the photoresist are substantially washed away while the developed portions of the photoresist layer remain as deposited. The developed, and thereby remaining portions of the photoresist layer thereupon cover the silicon thereby allowing for selected portions of the silicon layer to be etched. The etching acts on those uncovered portions of the silicon layers 6302 that correspond to the undeveloped regions of the photoresist layer. During etching, the developed portions of the photoresist layer 6304 cover, and protect, the covered portions of the silicon layer 6302, and

protect the covered portions of the silicon layer 6302 from the etchant. Following the etching, respective structures 6350 and 6352 remain that are ultimately used to form part of the respective optical (e.g., the input/output light coupler 112) and electronic (e.g., electronic portion 5101) portions.

Rewrite the heading on page 122, line 1 to read as follows.

#### VIII. Hybrid Active Electronic and Optical Circuits

Rewrite the paragraph that starts on page 124, line 23 and continues over to page 125, line 3 to read as follows.

FIG. 68 shows a side view of the hybrid active electronic and optical circuit 6502 such as shown in FIG. 66, during processing. The hybrid active electronic and optical circuit 6502 is formed on top of an SOI wafer 6600. The SOI wafer 6600 is initially formed with a planar upper surface. A photoresist layer 6804 is initially applied to the upper surface of the SOI wafer 6600. A photolithography mask is applied to the upper surface of the SOI wafer 6600 and the light is applied to the photolithography mask.

Rewrite the paragraph on page 125, that starts on line 4 and ends on line 9 to read as follows.

The purpose of the etching process using photolithography is to remove necessary portions of the upper most silicon layer in order to provide function of the passive optical component 6506, the active electronics portion 6504, the other electronic components 6602, and the other optical components 6604. The shape of the active electronic portion 6504, the other electronic components 6602, and the other optical components 6604 are shown in FIG. 66.

Rewrite the paragraph that starts on page 130, line 21 and continues over to page 131, line 3 to read as follows.

FIG. 70 shows another embodiment of hybrid active electronic and optical circuit 6502 as shown in FIG. 69, except that the waveguide prism 7002 has been incorporated in place of the waveguide grating 6902. Similarly, the waveguide prism 7002 is a passive device, that deflects the light being applied to the waveguide 6904 in a mode angle  $\theta_M$ . The use of the active electronic component 6504 allows adjustability of the light flowing through the waveguide prism 7002, thereby allowing light flowing through the waveguide prism 7002 to be controllably directed at a desired controllable angle to the waveguide 6904.

Rewrite the paragraph on page 132, that starts on line 7 and ends on line 15 to read as follows.

The Fabry-Perot cavity 7302 as shown in FIG. 73 represents another hybrid active electronic and optical circuit that may be formed on the silicon layer or an SOI wafer, and includes a plurality of passive optical portions 6506 and an active opto-electronic portion 6504.

The passive optical portion 6506 includes a waveguide 7310 and a plurality of gratings 7312. The gratings 7312 may be configured in a similar manner as Bragg gratings, surface gratings, or other known types of gratings. This Fabry-Perot waveguide operates similar to the well understood Fabry-Perot cavities used in optics. The reflectivity of mirrors (in this embodiment, the gratings act as mirrors) and the cavity optical length determine the reflection/transmission profile of the device.

Rewrite the paragraph that starts on page 133, line 22 and continues over to page 134, line 4 to read as follows.

The embodiment of grating 7304 shown in FIG. 75 is a passive device. In the Fabry-Perot cavity 7302 and the coupled Fabry-Perot cavity 7402 shown respectively in FIGS. 73 and 74, the respective active opto-electric portion 6504 is positioned between adjacent gratings 7304. It may be desired to provide a grating structure that is an active device. As such, the wavelengths of light that each grating could reflect or deflect could be controlled. FIGS. 77 and 76 show two alternate embodiments of active gratings 7602. The embodiments of gratings 7602 shown in FIGS. 76 and 77 thus are configured as hybrid active electronic and optical circuits 6502.

Rewrite the paragraph on page 135, that starts on line 1 and ends on line 13 to read as follows.

The upper silicon layer 6601 can be built up to the height equal to the raised lands 7502. Following this uniform build up of the upper silicon layer 6601, a uniform metalization layer can be applied across the entire upper surface of the upper silicon layer. At this time, the upper silicon layer will be thickened by the addition of silicon, and coated by a metal layer corresponding to the active electronic portion 6504. Those portions of the upper layers 6601 that do not correspond to the raised lands 7502 can have the upper middle layer etched away using known metal etching techniques. Following the etching away of the middle layer, the region of the upper silicon layers 6601 that are not coated by the remaining portions of the etched metal, i.e., the silicon areas corresponding to the lowered lands 7504, can be etched away using known silicon etching techniques. The etching of both the metal areas and the silicon layers utilizes masks that have openings, the regions of the openings corresponding either to the areas that are going to be etched or the areas that are not going to be etched.

Rewrite the paragraph on page 135, that starts on line 14 and ends on line 20 to read as follows.

In those embodiments of gratings 7602 in which silicon material 7620 is not added to the original upper silicon layer 6601, a metalized layer is added to the upper surface of the upper silicon layer 6601. The depth of the metal layer corresponds to the desired depth of the active electronic portion 6504. The techniques of etching away the metal layer of the active electronic portion 6504 and the underlying sacrificial silicon material of the upper silicon layer 6601 are similar to that described with respect to the removal of the metal and silicon portions where silicon has been added.



Rewrite the paragraph that starts on page 135, line 21 and continues over to page 136, line 3 to read as follows.

To fabricate the embodiment of the grating 7602 shown in FIG. 77, the entire upper silicon layer 6601 is built up to the desired height of the raised lands 7502. If the upper silicon layers are higher than the desired height of the raised lands 7502, then the entire upper silicon layer is etched uniformly down to the level of the raised lands 7502. Following the etching or metal deposition, it may be necessary to level the upper surface of the upper silicon layers using such means as, e.g., a chemical, mechanical polisher (CMP). Following the CMP processing, a photoresist is added to the upper surface of the upper silicon layer 6601.

Rewrite the paragraph on page 136, that starts on line 4 and ends on line 13 to read as follows.

Masks are used to define which area, depending upon the type of photoresist, are going to be etched away and light is applied through the apertures in the masks to the upper surface of the upper silicon layer 6601 to develop the photoresist, if necessary, to define which regions will be etched. Etching is then performed on the uncovered portions of the upper surface of the upper silicon layer 6601, until those uncovered portions are lowered to the level to the lower lands 7504. The upper surface of the lower lands 7504 are then coated with the metal layer corresponding to the active electronic portion 6504 of the grating. The deposition of the metal on the upper surface of the lower lands 7504 can be performed using a mask whose opening

corresponds to the regions of the upper silicon layers 6601 that have been etched down to the lower lands 7504.

Rewrite the paragraph on page 137, that starts on line 11 and ends on line 20.

FIG. 78 shows two gratings of the active chirped gratings regions 7806 being actuated, thereby diverting optical signals having wavelengths  $\lambda_1$  and  $\lambda_5$  to the passive chirped grating region 7814. Light having different wavelengths can thus be used to contain distinct data transmitted as optical signals. Data signals from the data electronic input portion 7816 may be applied to control the individual components of the active chirped grating region 7806. The data electronic input portion 7816 can be fabricated at the same time, on the chip, as the active electronic portions 6504 and the passive optical portion 6502 shown in the embodiments of FIGS. 76, 77 and 75 respectively. As such, the embodiment of wavelength division multiplexer modulator 7802 shown in FIG. 78 can be considered as an embodiment of hybrid active electronic and optical circuit 7602.

Rewrite the heading on page 141, line 4 to read as follows.

#### IX. Photonic Band Gap Device

Rewrite the paragraph on page 145, that starts on line 9 and ends on line 20 to read as follows.

FIG. 83 shows one embodiment of passive photonic band gap device (referred to as a shallow passive photonic band gap device 9010) whose region of photonic crystals is delineated by shallow pillars which do not extend through the entire vertical height of the waveguide. In one embodiment, the shallow passive pillars extend from the upper surface for a height  $h$ , but do not extend fully through the waveguide. Each one of the shallow passive pillars 9220 can be biased to control the relative dielectric constants of those areas of waveguide material set forth under the shallow passive pillars. In certain embodiments of shallow passive photonic band gap devices, the pillars are formed as wells, recesses, or indentations in the upper surface of the waveguide. FIG. 85 shows a top view of one embodiment of circular recesses that define the shape of the pillars. The pillars can also be defined by the square, rectangular, or some other regularly repeated shape, as opposed to circular holes.

Rewrite the heading on page 151, line 6 to read as follows.

X. Simulation Program For Hybrid Active Electronic and Optical Circuits

### REMARKS

Claims 12-38 are pending in the application. Claims 1-11 have been canceled. Claims 12-38 are newly added.

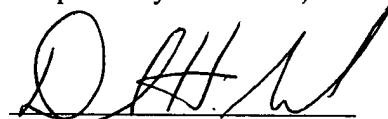
The present Preliminary Amendment seeks to correct several typographical errors in the specification discovered after filing of the parent application. It is respectfully submitted that no new matter has been introduced as a result of the amendments made herein.

In addition, applicant notes that there was an erroneous reference to Application Serial No. 09/859,593, in the domestic priority claim listed on page 1 of the parent application. In particular, applicant notes that the parent application, among other things, claims domestic priority to Application Serial No. 09/859,693, filed May 17, 2001. Applicant notes that the attached Declaration and Power of Attorney form correctly refers to Application Serial No. 09/859,693, filed May 17, 2001, in its priority claim; and a corresponding correction was previously made in the parent application. In addition, applicant notes that the attached Preliminary Amendment has modified the priority claim at page 1, line 6 of the application, so as to correctly refer to Application Serial No. 09/859,693 filed May 17, 2001.

An early and favorable office action is earnestly solicited.

The Commissioner is hereby authorized to charge any deficiency in the enclosed amount or credit any overpayment to Deposit Account No. 50-0310.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'D.H. Golub', written over a horizontal line.

Daniel H. Golub

Registration No. 33,701

MORGAN, LEWIS & BOCKIUS LLP  
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Philadelphia, PA 19103-2921  
215.963.5055

Dated: February 20, 2002

**SPECIFICATION WITH MARKINGS TO SHOW CHANGES MADE**

The title on page 1, that starts on line 1 and ends on line 2.

**HYBRID ACTIVE AND ELECTRONIC CIRCUIT WITH EVANESCENT COUPLING**

**[INTEGRATED OPTICAL/ELECTRONIC CIRCUITS AND ASSOCIATED METHODS  
OF SIMULTANEOUS GENERATION THEREOF]**

The paragraph on page 1, that starts on line 5 and ends on line 6.

This application is a continuation-in-part to U.S. Patent Application Serial No.  
09/859,693 [09/859,593], filed May 17, 2001.

The paragraph on page 4, that starts on line 17 and ends on line 22.

[FIG. 15, including ]FIGs. 15A to 15D[,] show side cross section views of the optical waveguide device of FIG. 13 or taken through sectional lines 15-15 in FIG. 13, FIG. 15A shows both gate electrodes 1304, 1306 being deactivated, FIG. 15B shows the gate electrode 1304 being actuated as the gate electrode 1306 is deactivated, FIG. 15C shows the gate electrode 1304 being deactuated as the gate electrode 1306 is activated, and FIG. 15D shows both gate electrodes 1304 and 1306 being actuated;

The paragraph on page 9, that starts on line 7 and ends on line 8.

[FIG. 63, including] FIGs. 63A to 63D[,] show[s] a method of fabricating the partially completed integrated optical/electronic circuit of FIG. 51;

The paragraph on page 9, that starts on line 9 and ends on line 10.

FIG. 64 [64A] shows a plot of intensity versus distance from a ledge of one embodiment of input/output light coupler 112 including a tapered gap portion;

The paragraph on page 9, that starts on line 11 and ends on line 12.

FIG. 65 [64B] shows another plot of intensity at a prism base for another embodiment of input/output light coupler having a prism, but without a tapered gap portion;

The paragraph on page 9, that starts on line 13 and ends on line 14.

[FIG. 64 shows the integrated optical/electronic circuit of FIG. 51 during a portion of the processing;]

The paragraph on page 9, that starts on line 15 and ends on line 16.

FIG. 66 [65] shows [a perspective view of] one embodiment of hybrid active electronic and optical circuit that is configured as a J-coupler;

The paragraph on page 9, that starts on line 17 and ends on line 18.

[FIG. 66 shows a top view of the hybrid active electronic and optical circuit of FIG. 65;]

The paragraph on page 9, that starts on line 21 and ends on line 21.

FIGs. 68A to 68D [FIG. 68] show[s] one embodiment of a method of anisotropically etching using a mask.

The paragraph on page 12, that starts on line 16 and ends on line 19.

Actual embodiments of discrete optical waveguide devices are described in the “Specific Embodiments of Optical Waveguide Device” portions of this disclosure. More complex optical circuits including a plurality of optical waveguide devices 100 [103] are described in the “Optical Circuits Including Optical Waveguide Devices” portion of this disclosure.

The paragraph on page 13, that starts on line 16 and ends on line 25.

FIGs. 51 to 52 [FIG. 1] show[s] one embodiment of an integrated optical/electric circuit 103. Multiple embodiments of integrated optical/electric circuit 103 are described herein as being formed using SOI devices, etc. The integrated optical/electric circuit can be configured with and combination of active optical, passive optical, active electronics, and passive components circuit. SOI technology is highly promising for integrated optical/electronic



circuits, and using relatively thin SOI devices (having an upper silicon layer less than 10  $\mu$ ) has many benefits. Using thin SOI devices for waveguides limits the vertical locations in which light can diffract, and therefor acts to localize the light to a relatively narrow waveguide. Thin SOI devices can be formed using planar lithography techniques including deposition and etching processes.

The paragraph that starts on page 16, line 10 and continues over to page 17, line 1.

The embodiments of optical waveguide device 100 shown in multiple figures including FIGs. 1-3, and 5, etc. include a field effect transistor (FET) portion 116 that is electrically coupled to a waveguide 106. One embodiment of the waveguide is fabricated proximate to, and underneath, the gate electrode of the FET portion 116. The waveguide 106 is typically made from silicon or another one or plurality of III-V semiconductors. The FET portion 116 includes a first body contact electrode 118, a gate electrode 120, and a second body contact electrode 122. A voltage can be applied by e.g., a voltage source 202 to one of the electrodes. The gate electrode 120 is the most common electrode in which the voltage level is varied to control the optical waveguide device. If the first body contact portion 118 and the second body contact portion are held at the same voltage by placing an electrical connector 204 there between, then the optical waveguide device 100 operates as a diode. If there is not an electrical connector between the first body contact portion 118 and the second body contact portion 122, then the optical waveguide device 100 acts as a transistor. This is true for each of the following FET/diode configurations. Whether any FET optical waveguide device 100 is biased to act as a transistor or diode, the optical waveguide device 100 is within the intended scope of the present

invention since either a diode or a transistor is capable of altering the effective mode index in the waveguide as described herein.

The paragraph on page 67, that starts on line 9 and ends on line 24.

FIG. 30 shows another embodiment of an optical waveguide device 100 including a grating 3008 that is used as a lens to focus light passing through the waveguide. The embodiment of optical waveguide device 100, or more particularly the FIG. 2 embodiment of gate electrode of the optical waveguide device, is modified by replacing the continuous gate electrode (in FIG. 2) with a discontinuous electrode in the shape of a grating (shown in FIG. 30). The grating 3008 is formed with a plurality of etchings 3010 that each substantially parallels the optical path 101 of the optical waveguide device. In the FIG. 30 embodiment of grating 3008, the thickness of the successive etchings 3010 to collectively form gate electrode 120 increases toward the center of the optical waveguide device, and decreases toward the edges 120a, 120b of the gate electrode 120. Therefore, the region of changeable propagation constant 190 in the waveguide is thicker at those regions near the center of the waveguide. Conversely, the region of changeable propagation constant 190 becomes progressively thinner at those regions of the waveguide near edges 120a, 120b. The propagation constant is a factor of both the volume and the shape of the material used to form the gate electrode. The propagation constant is thus higher for those regions of changeable propagation constant closer to the center of the waveguide.

The paragraph that starts on page 84, line 24 and continues over to page 85, line 10.

The high propagation constant bands 4502 correspond to the location of the input mirror gate electrodes 4402 or the output mirror gate electrodes 4404. The low propagation constant bands 4504 correspond to the bands between the input mirror gate electrodes 4402 or the output mirror gate electrodes 4404. The high propagation constant bands 4502 and the low propagation constant bands 4504 extend vertically through the waveguide. The input mirror gate electrodes 4402 and the output mirror gate electrodes 4404 can be shaped to provide, e.g., a concave mirror surface if desired. Additionally, deactuation of the input mirror gate electrodes 4402 or the output mirror gate electrodes 4404 removes any effect of the high propagation constant bands 4502 and low propagation constant bands 4504 from the waveguide of the resonator 4400. Such effects are removed since the propagation constant approaches a uniform level corresponding to 0 volts applied to the gate electrodes 4402, 4404 [4502, 4504].

The paragraph on page 89, that starts on line 17 and ends on line 23.

The wavelength separator 3902 acts to filter or modulate the wavelength of an incoming signal over waveguide 3916 into a plurality of light signals. Each of these light signals has a different frequency. Each of a plurality of waveguides 3918a to 3918d contain a light signal of different wavelength  $\lambda_1$  to  $\lambda_n$ , the wavelength of each signal corresponds to a prescribed limited bandwidth. For example, waveguide 3918a carries light having a color corresponding to wavelength  $\lambda_1$ , while waveguide 3918b carries a light having a color corresponding to wavelength  $\lambda_2$ , etc.

The heading on page 100, line 12.

## VI. [A] Generalization of Active Optical Devices in SOI

The heading on page 101, line 4.

## VII. INPUT/OUTPUT COUPLING EMBODIMENTS

The paragraph on page 105, that starts on line 5 and ends on line 19.

It is envisioned that the levels of silicon layers of the on-chip electronics portion 5101 are formed simultaneously with the one or more layers of the evanescent coupling region 5106, (or the gap portion ), and/or the light coupling portion 5110 of the input/output light coupler 112. In other words, any pair of vertically separated layers on the on-chip electronics portion 5101 may be formed simultaneously with any portion of optical elements 5106,[ 5108,] 5110 that is at substantially the same vertical level using, for example, planar lithography or projection lithography techniques. Therefore, any one of the one or more layers of the evanescent coupling region 5106 and/or the light coupling portion 5110 that are at generally the same vertical height as the layers on the electronics portion 5101 will be formed simultaneously, although the different portions will undergo different doping, masking, ion implantation, or other processes to provide the desired optical and/or electronic characteristics. As such, technology, know how, processing time, and equipment that has been developed relative to the fabrication of electronic circuits (e.g., techniques for fabricating thin SOI semiconductor chips) can be used to construct optical and electronic circuits simultaneously on the same substrate.

The paragraph on page 108, that starts on line 11 and ends on line 23.

The embodiment of input/output light coupler 112 shown in FIG. 55 includes a ledge 5502 that forms a support base for one edge of the light coupling portion 5110 (e.g., a prism or grating). The ledge 5502 may have thickness that provides the desired angle of the base of the [t he] input/output light coupler 112. The ledge 5502 is preferably formed by removing sacrificial material at the optical I/O location using an etching process, and the base of the light coupling portion 5110 is angled at a slight angle by resting it on the ledge 5502. In certain embodiments, the height of the ledge 5502 is in the range of under fifty microns, and may actually be in the range of one or a couple of microns. The gap portion 5106 may be filled with such optically clear polymer or glass material that provides the desired optical characteristics to the light entering into, or exiting from, the waveguide. Light rays 5120 passing through the embodiment of input/output light coupler 112, shown in the embodiment of FIG. 55, must satisfy the basic principles described relative to FIG. 51, e.g., equation 23.

The paragraph on page 112, that starts on line 8 and ends on line 24.

As light is exiting the output coupler from the waveguide, wherein the waveguide is carrying substantially uniform intensity of light across the cross-sectional area of the waveguide, it may be desired to once again convert the light exiting the output coupler into a light beam that has a Gaussian intensity profile. Evanescent couplings configured as a tapered gap portion 5106 as illustrated particularly in FIGS. 55 and 57, result in a closer fit to a Gaussian profile than

without the taper gap portion. For example, FIG. 64[A] shows the calculations for a 0.2 micron silicon waveguide formed with the taper. The tapered gap portion is illustrated by line 6402 in FIG. 64[A], and the height of the taper from the waveguide is illustrated along the right ordinate of FIG. 64[A]. An intensity profile curve 6406 is plotted to indicate the intensity profile at the base of the input/output light coupling device. The relative intensity value is plotted as the left ordinate in FIG. 64[A]. The abscissa measures the distance from a ledge (an arbitrary measuring point) in microns. A best fit Gaussian curve 6404 is plotted proximate the intensity profile 6406, to illustrate how effectively the output light from the output coupler models the Gaussian curve. FIG. 65 [64B] shows a similar curve as FIG. 64[A], except FIG. 65 [64B] models a constant thickness gap, as indicated by the fact that the taper curve 6410 is level in FIG. 65 [64B]. Curve 6412 of FIG. 65 measures the intensity profile for an output beam of light that is not Gaussian, but instead exponential.

The paragraph that starts on page 119, line 18 and continues over to page 120, line 6.

[FIG. 63, including ]FIGS. 63A [a] to 63D [d], show a process of simultaneously depositing silica, other suitable dielectric, polysilicon, etc. layer on both the light coupling portion 5110 and the electronic portion 5101. Initially, a silicon layer 6302 is deposited somewhat uniformly across the entire integrated optical/electrical circuit 103, including both the electronics portion 5101 and the light coupling portion 5110. Both the embodiments of the light coupling portion that may include prisms, as well as gratings, rely upon homogenous build up of silica throughout the entire light coupling portion. By comparison, the electronics portion 5101 is formed using a series of silica layers, interspersed with metallic interconnects through which

metallic vias vertically extend. Therefore, a series of additional metalization and other steps are necessary between successive depositions of silica. By comparison, since the light coupling portion is homogenous, relatively little processing will occur between the various silica deposition steps. In FIG. 63A, the layer of silicon 6302 is deposited on the upper surface of the integrated optical/electrical circuit 103 using known silicon deposition techniques, such as chemical vapor deposition and sputtering.

The paragraph on page 120, that starts on line 7 and ends on line 15.

The planer lithography method continues in FIG. 63B [b] in which a photoresist layer 6304 is deposited on the upper surface of the deposited silicon layer 6302. Photoresist may be applied, and then the substrate 102 typically spun so that the photoresist layer is extended under the influence of centrifugal force to a substantially uniform thickness. In FIG. 63C, the lithography portion 6308 selectively applies light to the upper surface of the photoresist layer 6304, thereby acting to develop certain regions of the photoresist layer. Depending upon the type of photoresist, the photoresist may harden either if light is applied to it, or will not harden if light is not applied. The lithography portion 6308 includes a lithography light source 6310 and a lithography mask 6312.

The paragraph that starts on page 120, line 23 and continues over to page 121, line 8.

The photoresist layer 6304 is then washed, in which the undeveloped portions of the photoresist are substantially washed away while the developed portions of the photoresist layer

remain as deposited. The developed, and thereby remaining portions of the photoresist layer thereupon cover the silicon thereby allowing for selected portions of the silicon layer to be etched. The etching acts on those uncovered portions of the silicon layers 6302 that correspond to the undeveloped regions of the photoresist layer. During etching, the developed portions of the photoresist layer 6304 cover, and protect, the covered portions of the silicon layer 6302, and protect the covered portions of the silicon layer 6302 from the etchant. Following the etching, respective structures 6350 [6450] and 6352 [6452] remain that are ultimately used to form part of the respective optical (e.g., the input/output light coupler 112) and electronic (e.g., electronic portion 5101) portions.

The heading on page 122, that starts on line 1.

#### VIII. Hybrid Active Electronic and Optical Circuits

The paragraph that starts on page 124, line 23 and continues over to page 125, line 3.

FIG. 68 [66] shows a side [top] view of the hybrid active electronic and optical circuit 6502 such as shown in FIG. 66 [65], during processing. The hybrid active electronic and optical circuit 6502 is formed on top of an SOI wafer 6600. The SOI wafer 6600 is initially formed with a planar upper surface. A photoresist layer 6804 is initially applied to the upper surface of the SOI wafer 6600. A photolithography mask is applied to the upper surface of the SOI wafer 6600 and the light is applied to the photolithography mask.



The paragraph on page 125, that starts on line 4 and ends on line 9.

The purpose of the etching process using photolithography is to remove necessary portions of the upper most silicon layer in order to provide function of the passive optical component 6506, the active electronics portion 6504, the other electronic components 6602, and the other optical components 6604. The shape of the active electronic portion 6504, the other electronic components 6602, and the other optical components 6604 are shown in FIG. 66 [block].

The paragraph that starts on page 130, line 21 and continues over to page 131, line 3.

FIG. 70 shows another embodiment of hybrid active electronic and optical circuit 6502 as shown in FIG. 69, except that the waveguide prism 7002 has been incorporated in place of the waveguide grating 6902. Similarly, the waveguide prism 7002 is a passive device, that deflects the light being applied to the waveguide 6904 in a mode angle  $\theta_M$ . The use of the active electronic component 6504 allows adjustability of the light flowing through the waveguide prism 7002, thereby allowing light flowing through the waveguide prism 7002 to be controllably directed at a desired controllable angle to the waveguide 6904.

The paragraph on page 132, that starts on line 7 and ends on line 15.

The Fabry-Perot cavity 7302 as shown in FIG. 73 represents another hybrid active electronic and optical circuit that may be formed on the silicon layer or an SOI wafer, and

includes a plurality of passive optical portions 6506 [7506] and an active opto-electronic portion 6504. The passive optical portion 6506 includes a waveguide 7310 and a plurality of gratings 7312. The gratings 7312 may be configured in a similar manner as Bragg gratings, surface gratings, or other known types of gratings. This Fabry-Perot waveguide operates similar to the well understood Fabry-Perot cavities used in optics. The reflectivity of mirrors (in this embodiment, the gratings act as mirrors) and the cavity optical length determine the reflection/transmission profile of the device.

The paragraph that starts on page 133, line 22 and continues over to page 134, line 4.

The embodiment of grating 7304 shown in FIG. 75 is a passive device. In the Fabry-Perot cavity 7302 and the coupled Fabry-Perot cavity 7402 shown respectively in FIGS. 73 and 74, the respective active opto-electric portion 6504 [6502] is positioned between adjacent gratings 7304. It may be desired to provide a grating structure that is an active device. As such, the wavelengths of light that each grating could reflect or deflect could be controlled. FIGS. 77 [75] and 76 show two alternate embodiments of active gratings 7602. The embodiments of gratings 7602 shown in FIGS. 76 and 77 thus are configured as hybrid active electronic and optical circuits 6502.

The paragraph on page 135, that starts on line 1 and ends on line 13.

The upper silicon layer 6601 can be built up to the height equal to the raised lands 7502. Following this uniform build up of the upper silicon layer 6601, a uniform metalization layer can

be applied across the entire upper surface of the upper silicon layer. At this time, the upper silicon layer will be thickened by the addition of silicon, and coated by a metal layer corresponding to the active electronic portion 6504. Those portions of the upper layers 6601 that do not correspond to the raised lands 7502 can have the upper middle layer etched away using known metal etching techniques. Following the etching away of the middle layer, the region of the upper silicon layers 6601 [7601] that are not coated by the remaining portions of the etched metal, i.e., the silicon areas corresponding to the lowered lands 7504, can be etched away using known silicon etching techniques. The etching of both the metal areas and the silicon layers utilizes masks that have openings, the regions of the openings corresponding either to the areas that are going to be etched or the areas that are not going to be etched.

The paragraph on page 135, that starts on line 14 and ends on line 20.

In those embodiments of gratings 7602 in which silicon material 7620 is not added to the original upper silicon layer 6601 [7601], a metalized layer is added to the upper surface of the upper silicon layer 6601 [7601]. The depth of the metal layer corresponds to the desired depth of the active electronic portion 6504. The techniques of etching away the metal layer of the active electronic portion 6504 and the underlying sacrificial silicon material of the upper silicon layer 6601 [7601] are similar to that described with respect to the removal of the metal and silicon portions where silicon has been added.

The paragraph that starts on page 135, line 21 and continues over to page 136, line 3.

To fabricate the embodiment of the grating 7602 shown in FIG. 77, the entire upper silicon layer 6601 [7601] is built up to the desired height of the raised lands 7502. If the upper silicon layers are higher than the desired height of the raised lands 7502, then the entire upper silicon layer is etched uniformly down to the level of the raised lands 7502. Following the etching or metal deposition, it may be necessary to level the upper surface of the upper silicon layers using such means as, e.g., a chemical, mechanical polisher (CMP). Following the CMP processing, a photoresist is added to the upper surface of the upper silicon layer 6601 [7601].

The paragraph on page 136, that starts on line 4 and ends on line 13.

Masks are used to define which area, depending upon the type of photoresist, are going to be etched away and light is applied through the apertures in the masks to the upper surface of the upper silicon layer 6601 [7601] to develop the photoresist, if necessary, to define which regions will be etched. Etching is then performed on the uncovered portions of the upper surface of the upper silicon layer 6601 [7601], until those uncovered portions are lowered to the level to the lower lands 7504. The upper surface of the lower lands 7504 are then coated with the metal layer corresponding to the active electronic portion 6504 of the grating. The deposition of the metal on the upper surface of the lower lands 7504 can be performed using a mask whose opening corresponds to the regions of the upper silicon layers 6601 [7601] that have been etched down to the lower lands 7504.

The paragraph on page 137, that starts on line 11 and ends on line 20.

FIG. 78 shows two gratings of the active chirped gratings regions 7806 being actuated, thereby diverting optical signals having wavelengths  $\lambda_1$  and  $\lambda_5$  to the passive chirped grating region 7814. Light having different wavelengths can thus be used to contain distinct data transmitted as optical signals. Data signals from the data electronic input portion 7816 may be applied to control the individual components of the active chirped grating region 7806. The data electronic input portion 7816 can be fabricated at the same time, on the chip, as the active electronic portions 6504 and the passive optical portion 6502 shown in the embodiments of FIGS. 76, [and ]77 and 75 respectively. As such, the embodiment of wavelength division multiplexer modulator 7802 shown in FIG. 78 can be considered as an embodiment of hybrid active electronic and optical circuit 7602.

The heading on page 141, line 4.

#### IX. [IIIV.] Photonic Band Gap Device

The paragraph on page 145, that starts on line 9 and ends on line 20.

FIG. 83 shows one embodiment of passive photonic band gap device (referred to as a shallow passive photonic band gap device 9010) whose region of photonic crystals is delineated by shallow pillars which do not extend through the entire vertical height of the waveguide. In one embodiment, the shallow passive pillars extend from the upper surface for a height  $h$ , but do not extend fully through the waveguide. Each one of the shallow passive pillars 9220 can be biased to control the relative dielectric constants of those areas of waveguide material set forth

under the shallow passive pillars. In certain embodiments of shallow passive photonic band gap devices, the pillars are formed as wells, recesses, or indentations in the upper surface of the waveguide. FIG. 85 [87] shows a top view of one embodiment of circular recesses that define the shape of the pillars. The pillars can also be defined by the square, rectangular, or some other regularly repeated shape, as opposed to circular holes.

The heading on page 151, line 6.

X. [IX.]      Simulation Program For Hybrid Active Electronic and Optical Circuits